FORM PTO-1449 (Modified) (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. TI-32068 (032350.B324)	APPLICATION NO. 09/960,348
	LIST OF REFERENCES CITED BY APPLICANT (Use several sheets if necessary)	APPLICANT Kaoru Awaka et al.	
		FILING DATE September 24, 2001	GROUP Not yet known

[PTO stamp: FEB 0 4 2002]

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

[stamp: RECEIVED FEB 0 6 2002 Technology Center 2100]

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

(✓)		A 4.4 ns CMOS 54x54-b Multiplier Using Pass-Transistor Multiplexer, IEEE Journal of Solid-State Circuits, Vol. 30, No.3, March 1995
(✓)		TWTXBB: A Low Latency, High Thoroughput Multiplier Architecture Using a New 4-2 Compressor, 7th International Conference on VLSI Design, January 1994
(✓)		A 0.25-μm CMOS 0.9-V 100-MHz DSP Core, IEEE Journal of D-State Circuits, Vol. 32 No. 1. January 1997

EXAMINER Ngo	DATE CONSIDERED 4/14/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

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							YES	NO

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℮		Design of high-speed low power 3-2 counter and 4-2 compressor for fast multipliers, Electronics Letters, vol. 34 No.4, February 19, 1998

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